CLAIMS

1. An image rejection mixer, comprising:

a first mixer that receives an RF input signal and a first local oscillator (LO) signal and generates a first intermediate frequency (IF) output signal, wherein the first LO signal is sin $\omega_{lo}t$;

a second mixer that receives the RF input signal and a second LO signal and generates a second IF output signal, wherein the second LO signal is -cos $\omega_{lo}t$, and wherein $\omega_{lo}t$ is a frequency signal generated by a local oscillator; and

a summer connected to the first and second mixers for receiving the first and second IF output signals and generating a combined IF output signal.

2. The image rejection mixer of claim 1, further comprising a phase shift circuit connected between the first mixer and the summer, the phase shift circuit receiving the first IF output signal and generating a phase lag signal, wherein the phase lag signal is provided to the summer to be combined with the second IF output signal.

3. The image rejection mixer of claim 2, wherein the phase shift circuit causes the phase lag signal to lag the first IF output signal by about 90 degrees.

4. The image rejection mixer of claim 1, wherein the first and second mixers are differential circuits.

5. The image rejection mixer of claim 1, further comprising:

a Q limiter circuit connected to the first mixer, the Q limiter circuit receiving an $LO_Q$ signal from the local oscillator and generating the first LO signal therefrom; and

an I limiter circuit connected to the second mixer, the I limiter circuit receiving an $LO_I$ signal from the local oscillator and generating the second LO signal therefrom.

6. The image rejection mixer of claim 5, wherein the I limiter circuit receives an injection enable signal for selecting between a high side LO injection and a low side LO injection.

7. The image rejection mixer of claim 6, wherein the Q limiter circuit comprises:

a first current source having a first terminal connected to ground and a second terminal;

a first transistor and a second transistor, the emitters of the first and second transistors being connected together and to the second terminal of the first current source, and the bases of the first and second transistors receiving the $LO_Q$ signal;

a second current source having a first terminal connected to ground and a second terminal;

a third transistor and a fourth transistor, the emitters of the third and fourth transistors being connected together and to the second terminal of the second current source, and the bases of the third and fourth transistors receiving the $LO_Q$ signal, wherein the collectors of the first and third transistors are connected together at a first node, the collectors of the second and fourth transistors are connected together at a second node, and the bases of the second and third transistors are connected together at a third node;

a first resistor having a first terminal connected to the first node and a second terminal; and

a second resistor having a first terminal connected to the second node and a second terminal connected to the second terminal of the first resistor, wherein the first LO signal is a differential signal obtained at the first and second nodes.

8. The image rejection mixer of claim 7, wherein the first current source is always disabled and the second current source is always enabled.

9. The image rejection mixer of claim 6, wherein the I limiter circuit comprises:

a first current source having a first terminal connected to ground and a second terminal;

a first transistor and a second transistor, the emitters of the first and second transistors being connected together and to the second terminal of the first current source, and the bases of the first and second transistors receiving the $LO_I$ signal;

a second current source having a first terminal connected to ground and a second terminal;

a third transistor and a fourth transistor, the emitters of the third and fourth transistors being connected together and to the second terminal of the second current source, and the bases of the third and fourth transistors receiving the $LO_Q$ signal, wherein the collectors of the first and third transistors are connected together at a first node, the collectors of the second and fourth transistors are connected together at a second node, and the bases of the second and third transistors are connected together at a third node;

a first resistor having a first terminal connected to the first node and a second terminal; and

a second resistor having a first terminal connected to the second node and a second terminal connected to the second terminal of the first resistor, wherein the second LO signal is a differential signal obtained at the first and second nodes.

10. The image rejection mixer of claim 9, wherein the first current source is enabled by the injection enable signal for high side LO injection and the second current source is enabled by the injection enable signal for low side LO injection.

11. An image rejection mixer with a switchable high or low side local oscillator (LO) injection, the image rejection mixer comprising:

a Q mixer that receives an RF input signal and a first local oscillator (LO) signal and generates a first intermediate frequency (IF) output signal;

a Q limiter circuit connected to the Q mixer, the Q limiter circuit receiving an $LO_Q$ signal from the local oscillator and generating the first LO signal therefrom, wherein the $LO_Q$ signal is sin $\omega_{lo}t$;

an I mixer that receives the RF input signal and a second LO signal and generates a second IF output signal;

an I limiter circuit connected to the I mixer, the I limiter circuit receiving an $LO_I$ signal from the local oscillator and generating the second LO signal therefrom, wherein the $LO_I$ signal is -cos $\omega_{lo}t$, $\omega_{lo}t$ is a frequency signal generated by a local oscillator, and wherein the I limiter circuit receives an injection enable signal for switching between the high side LO injection and the low side LO injection;

a phase shift circuit connected to the Q mixer and receiving the first IF output signal and generating a phase

lag signal that lags the first IF output signal by about 90 degrees; and

a summer connected to the phase shift circuit and the I mixer for receiving the phase lag signal and the second IF output signal and generating a combined IF output signal.

12. The image rejection mixer of claim 11, wherein the Q limiter circuit comprises:

a first current source having a first terminal connected to ground and a second terminal;

a first transistor and a second transistor, the emitters of the first and second transistors being connected together and to the second terminal of the first current source, and the bases of the first and second transistors receiving the $LO_Q$ signal;

a second current source having a first terminal connected to ground and a second terminal;

a third transistor and a fourth transistor, the emitters of the third and fourth transistors being connected together and to the second terminal of the second current source, and the bases of the third and fourth transistors receiving the $LO_Q$ signal, wherein the collectors of the first and third transistors are connected together at a first node, the collectors of the second and fourth transistors are connected together at a second node, and the bases of the second and third transistors are connected together at a third node;

a first resistor having a first terminal connected to the first node and a second terminal; and

a second resistor having a first terminal connected to the second node and a second terminal connected to the second terminal of the first resistor, wherein the first LO signal is a differential signal obtained at the first and second nodes.

13. The image rejection mixer of claim 12, wherein the first current source is always disabled and the second current source is always enabled.

14. The image rejection mixer of claim 13, wherein the I limiter circuit comprises:

a third current source having a first terminal connected to ground and a second terminal;

a fifth transistor and a sixth transistor, the emitters of the fifth and sixth transistors being connected together and to the second terminal of the third current source, and the bases of the fifth and sixth transistors receiving the $LO_I$ signal;

a fourth current source having a first terminal connected to ground and a second terminal;

a seventh transistor and an eighth transistor, the emitters of the seventh and eighth transistors being connected together and to the second terminal of the fourth current source, and the bases of the seventh and eighth transistors receiving the $LO_I$ signal, wherein the collectors of the fifth and seventh transistors are connected together at a fourth node, the collectors of the sixth and eighth transistors are connected together at a fifth node, and the bases of the sixth and seventh transistors are connected together at a sixth node;

a third resistor having a first terminal connected to the third node and a second terminal; and

a fourth resistor having a first terminal connected to the fifth node and a second terminal connected to the second terminal of the third resistor, wherein the second LO signal is a differential signal obtained at the fourth and fifth nodes.

15. The image rejection mixer of claim 14, wherein the third current source is enabled by the injection enable signal for high side LO injection and the fourth current source is enabled by the injection enable signal for low side LO injection.

16. A quadrature limiter circuit comprising:

an I limiter circuit including an I limiter first side and an I limiter second side, wherein the I limiter first side is a phase inverting side and the I limiter second side is a phase non-inverting side, the I limiter circuit receiving a first local oscillator (LO) signal and generating a pair of I limiter output signals, wherein an injection enable signal is provided to the I limiter first and second sides for selectively enabling one of the I limiter first and second sides; and

a Q limiter circuit including a Q limiter first side and a Q limiter second side, the Q limiter circuit receiving a second local oscillator (LO) signal and generating a pair of Q limiter output signals, wherein the Q limiter first side is always disabled and the Q limiter second side is always enabled.

17. The quadrature limiter circuit of claim 16, wherein the Q limiter circuit comprises:

a first current source having a first terminal connected to ground and a second terminal;

a first transistor and a second transistor, the emitters of the first and second transistors being connected together and to the second terminal of the first current source, and the bases of the first and second transistors receiving the second LO signal;

a second current source having a first terminal connected to ground and a second terminal;

a third transistor and a fourth transistor, the emitters of the third and fourth transistors being connected together and to the second terminal of the second current source, and the bases of the third and fourth transistors receiving the first LO signal, wherein the collectors of the first and third transistors are connected together at a first node, the collectors of the second and fourth transistors are connected together at a second node, and the bases of the second and third transistors are connected together at a third node;

a first resistor having a first terminal connected to the first node and a second terminal; and

a second resistor having a first terminal connected to the second node and a second terminal connected to the second terminal of the first resistor, wherein the pair of Q limiter output signals is obtained at the first and second nodes.

18. The image rejection mixer of claim 17, wherein the first current source is always disabled and the second current source is always enabled.

19. The quadrature limiter circuit of claim 18, further comprising:

an I mixer circuit connected to the I limiter circuit, the I mixer circuit receiving an RF input signal and the pair of I limiter output signals, and generating a first intermediate frequency (IF) signal therefrom; and

a Q mixer circuit connected to the Q limiter circuit, the Q mixer circuit receiving the RF input signal and the pair of Q limiter output signals, and generating a second IF signal therefrom.

20. The quadrature limiter circuit of claim 16, wherein the first LO signal received by the I limiter circuit comprises $-\cos \omega_{lo}t$, the second LO signal received by the Q

limiter circuit comprises sin $\omega_{lo}t$, and wherein $\omega_{lo}t$ is a frequency signal generated by a local oscillator.

21. A method of generating an intermediate frequency (IF) signal from a radio frequency (RF) signal, the method comprising the steps of:

mixing an RF input signal and a first local oscillator (LO) signal to generate a first intermediate frequency (IF) output signal, wherein the first LO signal is sin $\omega_{lo}t$;

mixing the RF input signal and a second LO signal to generate a second IF output signal, wherein the second LO signal is -cos $\omega_{lo}t$, and wherein $\omega_{lo}t$ is a frequency signal generated by a local oscillator; and

summing the first and second IF output signals to generate a combined IF output signal.

22. The method of generating an IF signal of claim 21, further comprising the step of:

phase shifting the first IF output signal to generate a phase lag signal and combining the phase lag signal with the second IF signal in the summing step to generate the combined IF output signal.

23. The method of generating an IF signal of claim 22, further comprising the step of:

performing one of high side injection and low side injection on the first LO signal in accordance with a value of an injection enable signal prior to mixing the first LO signal with the RF signal to generate the first IF output signal.